

The safety support in the NVIDIA IGX™ platform includes:

- IGX Thor supports two software safety architectures:

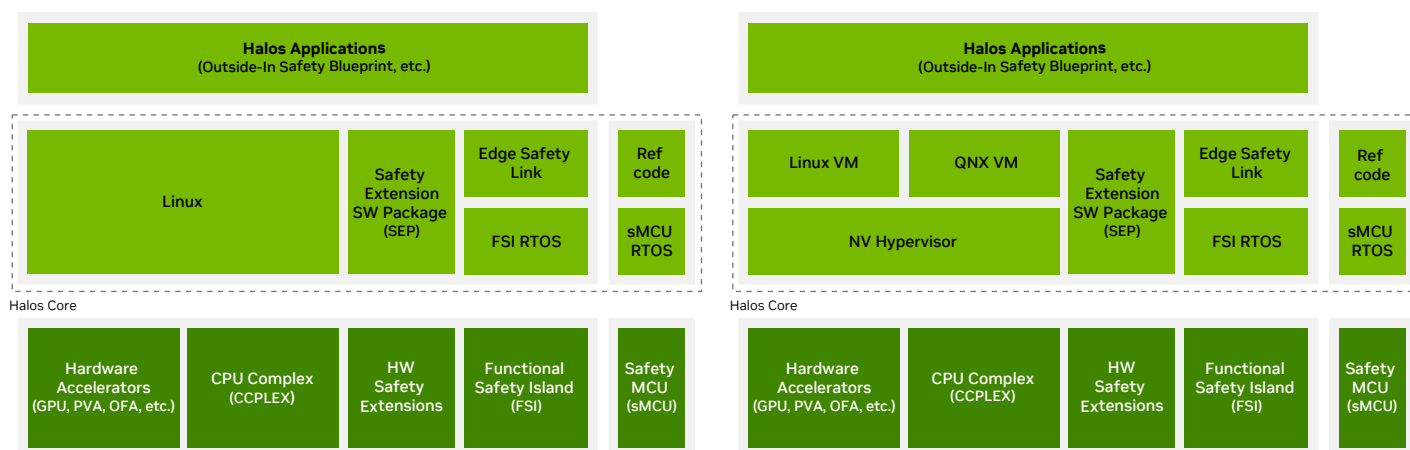
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- The diagram illustrates the SR Architecture, showing the flow of data and control between various components. The architecture is organized into several layers and functional blocks:
- Top Layer (Inputs/Outputs):**
 - SR Sensor(s)/Input(s)** (Green box) provides input to the **AI/ML Single-Channel Safety Function** and the **Safety Monitor**.
 - SR Final Element(s) Network Slaves** (Green box) receives output from the **Safety MCU (sMCU)**.
 - Processing and Safety Layers:**
 - AI/ML Single-Channel Safety Function** (Grey box) and **Safety Monitor** (Grey box) are part of the initial processing.
 - Network Master** (Grey box) is connected to the **Safety Monitor** and the **Safety Decision Engine**.
 - Safety Decision Engine** (Grey box) and **Safety Network Master** (Grey box) are part of the decision-making layer.
 - Edge Safety Link** (Green box) and **FSI RTOS** (Green box) are part of the communication and real-time operating system layer.
 - Ref code** (Green box) and **sMCU RTOS** (Green box) are part of the reference code and real-time operating system layer.
 - Safety MCU (sMCU)** (Green box) is the final output component.
 - Virtualization and Hardware Layers:**
 - Linux VM** (Green box) and **NV Hypervisor** (Green box) are part of the virtualization layer.
 - HW Safety Extensions** (Green box) and **Functional Safety Island (FSI)** (Green box) are part of the hardware safety extensions layer.
 - Hardware Accelerators:**
 - Hardware Accelerators (GPU, PVA, OFA, ...)** (Green box) are part of the hardware acceleration layer.
 - Central Processing:**
 - CPU Complex (CCPLEX)** (Green box) is the central processing unit.
- The diagram uses color coding: Green boxes represent the main functional blocks, Grey boxes represent safety and decision-making components, and White boxes represent the underlying hardware and virtualization layers. Arrows indicate the flow of data and control between these components.

NVIDIA IGX Functional Safety Support

SoC Safety Extensions	Halos Core SEP	Edge Safety Link	Safety Collaterals
> DRAM ECC > Temperature, clock, and voltage monitoring > ARM RAS > Hardware safety extensions > IST (In System Test) > FSI (Functional Safety Island) > Support for Freedom From Interference (FFI)	> Drivers for IST (In System Test) > Hardware Safety Manager and Error Collator for monitoring and collating error signals > Error Propagation to FSI and NVIDIA IGX sMCU > Diagnostic monitoring, including Safe State and FuSa State monitoring and heartbeat mechanism at various layers	> A safe and secure interface between IGX and safety-related elements, such as safety-related sensors and actuators > The infrastructure on which safety protocols such as FSOE, PROFIsafe, or CIP Safety can be implemented	> IGX Thor in Safety-Related Systems Application Note, including how to address standards such as IEC 61508, ISO 13849, ISO 25119, ISO/IEC TS 22440, DO178C, and DO254 > Safety Manual and FMEDA > Inspection report by TUV Rheinland

Safety Architecture Examples

Additional examples available in IGX Thor in the Safety-Related Systems Application Note.



NVIDIA IGX Functional Safety Support Summary

- > **Avoidance of systematic failures in hardware.** The process with which IGX SoC has been developed is compliant with ISO 26262 up to ASIL D and compatible up to IEC 61508 SIL 3/SC 3.
- > **Avoidance of systematic failures in software.** The process with which Halos Core for IGX has been developed (named “NVIDIA PLC-L3”) is compliant with ISO 26262 up to ASIL D and compatible up to IEC 61508 SIL 3/SC 3.
- > **Detection and control of random hardware failures.** Thor SoC meets the applicable ISO 26262 requirements for random hardware integrity of ASIL B and compatible up to IEC 61508 SIL 2 (SIL 3 for Safety Island).

Ready to Get Started?

[Learn more](#) about NVIDIA Halos for robotics.